查询STM690A供应商

STM706T/S/R, STM706P, STM708T/S/R

3V Supervisor

FEATURES SUMMARY

- PRECISION V_{CC} MONITOR
  - STM706/708
    T: 3.00V ≤ V_{RST} ≤ 3.15V
    S: 2.88V ≤ V_{RST} ≤ 3.00V
    R; STM706P: 2.59V ≤ V_{RST} ≤ 2.70V
- RST AND $\overline{RST}$ OUTPUTS
- 200ms (TYP) t_{rec}
- WATCHDOG TIMER - 1.6sec (TYP)
- MANUAL RESET INPUT ($\overline{MR}$)
- POWER-FAIL COMPARATOR (PFI/$\overline{PFO}$)
- LOW SUPPLY CURRENT - 40µA (TYP)
- GUARANTEED $\overline{RST}$ (RST) ASSERTION DOWN TO V_{CC} = 1.0V
- OPERATING TEMPERATURE:
  –40°C to 85°C (Industrial Grade)

Figure 1. Packages

SO8 (M)

TSSOP8 3x3 (DS)

Table 1. Device Options

	Watchdog Input	Watchdog Output	Active-Low $\overline{RST}$(1)	Active-High RST(1)	Manual Reset Input	Power-fail Comparator
STM706T/S/R	✔	✔	✔		✔	✔
STM706P(2)	✔	✔		✔	✔	✔
STM708T/S/R			✔	✔	✔	✔

Note: 1. Push-Pull Output
2. The STM706P is identical to the STM706R, except its reset output is active-high.

TABLE OF CONTENTS

FEATURES SUMMARY 1
Figure 1. Packages 1
Table 1. Device Options 1

SUMMARY DESCRIPTION 4
Figure 2. Logic Diagram (STM706T/S/R and STM706P) 4
Figure 3. Logic Diagram (STM708T/S/R) 4
Table 2. Signal Names 4
Figure 4. STM706T/S/R and STM706P SO8 Connections 5
Figure 5. STM706T/S/R and STM706P TSSOP8 Connections 5
Figure 6. STM708T/S/R SO8 Connections 5
Figure 7. STM708T/S/R TSSOP8 Connections 5
Pin Descriptions 6
Table 3. Pin Description 6
Figure 8. Block Diagram (STM706T/S/R and STM706P) 7
Figure 9. Block Diagram (STM708T/S/R) 7
Figure 10. Hardware Hookup 8

OPERATION 9
Reset Output 9
Push-button Reset Input 9
Watchdog Input (STM706T/S/R and STM706P) 9
Watchdog Output (STM706T/S/R and STM706P) 9
Power-fail Input/Output 9
Ensuring a Valid Reset Output Down to V_{CC} = 0V 9
Figure 11. Reset Output Valid to Ground Circuit 9
Interfacing to Microprocessors with Bi-directional Reset Pins 10
Figure 12. Interfacing to Microprocessors with Bi-directional Reset I/O 10

TYPICAL OPERATING CHARACTERISTICS 10
Figure 13. Supply Current vs. Temperature (no load) 10
Figure 14. V_{PFI} Threshold vs. Temperature 11
Figure 15. Reset Comparator Propagation Delay vs. Temperature 11
Figure 16. Power-up t_{rec} vs. Temperature 12
Figure 17. Normalized Reset Threshold vs. Temperature 12
Figure 18. Watchdog Time-out Period vs. Temperature 13
Figure 19. PFI to $\overline{PFO}$ Propagation Delay vs. Temperature 13
Figure 20. Output Voltage vs. Load Current (V_{CC} = 5V; V_{BAT} = 2.8V; T_A = 25°C) 14
Figure 21. Output Voltage vs. Load Current (V_{CC} = 0V; V_{BAT} = 2.8V; T_A = 25°C) 14
Figure 22. $\overline{RST}$ Output Voltage vs. Supply Voltage 15
Figure 23. RST Output Voltage vs. Supply Voltage 15
Figure 24. Power-fail Comparator Response Time (Assertion) 16
Figure 25. Power-fail Comparator Response Time (De-Assertion) 16

Figure 26.Maximum Transient Duration vs. Reset Threshold Overdrive 17

MAXIMUM RATING 17

Table 4. Absolute Maximum Ratings 17

DC and AC PARAMETERS 18

Table 5. Operating and AC Measurement Conditions 18
Figure 27.AC Testing Input/Output Waveforms 18
Figure 28.Power-fail Comparator Waveform 18
Figure 29.$\overline{MR}$ Timing Waveform 19
Figure 30.Watchdog Timing (STM706T/S/R and STM706P) 19
Table 6. DC and AC Characteristics 19

PACKAGE MECHANICAL 21

Figure 31.SO8 – 8-lead Plastic Small Outline, 150 mils body width, Package Mechanical. 21
Table 7. SO8 – 8-lead Plastic Small Outline, 150 mils body width, Package Mechanical Data . . 21
Figure 32.TSSOP8 – 8-lead, Thin Shrink Small Outline, 3x3mm body size, Outline 22
Table 8. TSSOP8 – 8-lead, Thin Shrink Small Outline, 3x3mm body size, Mechanical Data 22

PART NUMBERING 23

Table 9. Ordering Information Scheme 23
Table 10. Marking Description 24

REVISION HISTORY 25

Table 11. Document Revision History 25

SUMMARY DESCRIPTION

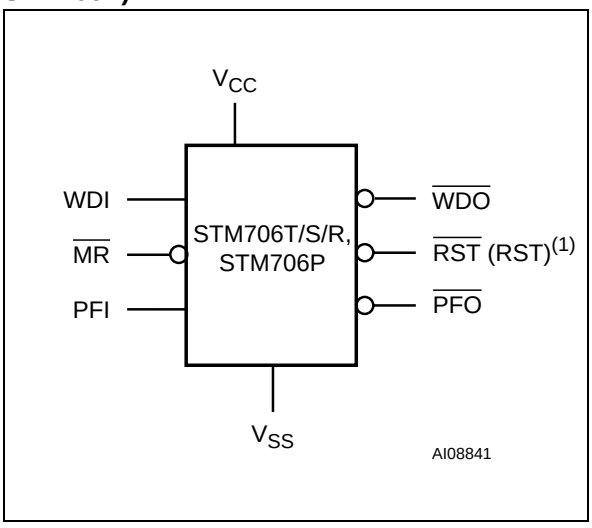
The STM70x Supervisors are self-contained devices which provide microprocessor supervisory functions. A precision voltage reference and comparator monitors the V_{CC} input for an out-of-tolerance condition. When an invalid V_{CC} condition occurs, the reset output ($\overline{RST}$) is forced low (or high in the case of RST).

These devices also offer a watchdog timer (except for STM708T/S/R) as well as a power-fail comparator to provide the system with an early warning of impending power failure.

The STM706P is identical to the STM706R, except its reset output is active-high.

These devices are available in a standard 8-pin SOIC package or a space-saving 8-pin TSSOP package.

Figure 2. Logic Diagram (STM706T/S/R and STM706P)



Note: 1. For STM706P only.

Figure 3. Logic Diagram (STM708T/S/R)

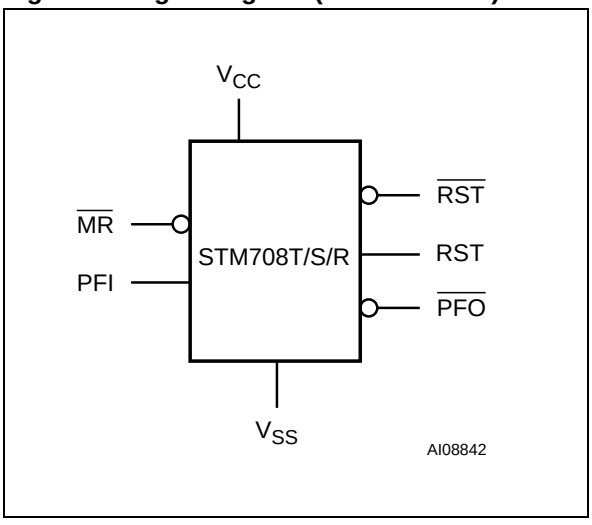
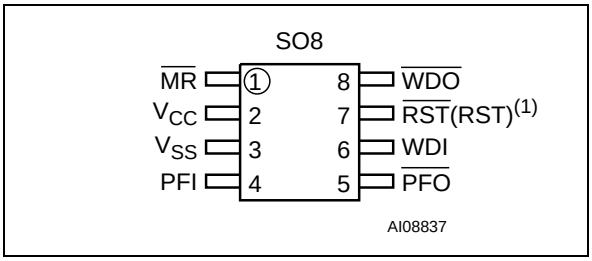


Table 2. Signal Names

$\overline{MR}$	Push-button Reset Input
WDI	Watchdog Input
$\overline{WDO}$	Watchdog Output
$\overline{RST}$	Active-Low Reset Output
RST(1)	Active-High Reset Output
V_{CC}	Supply Voltage
PFI	Power-fail Input
$\overline{PFO}$	Power-fail Output
V_{SS}	Ground
NC	No Connect

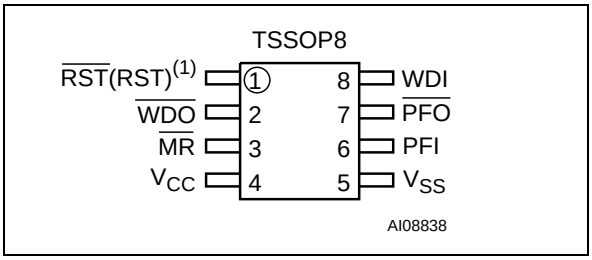
Note: 1. For STM706P and STM708T/S/R only.

Figure 4. STM706T/S/R and STM706P SO8 Connections



Note: 1. For STM706P reset output is active-high.

Figure 5. STM706T/S/R and STM706P TSSOP8 Connections



Note: 1. For STM706P reset output is active-high.

Figure 6. STM708T/S/R SO8 Connections

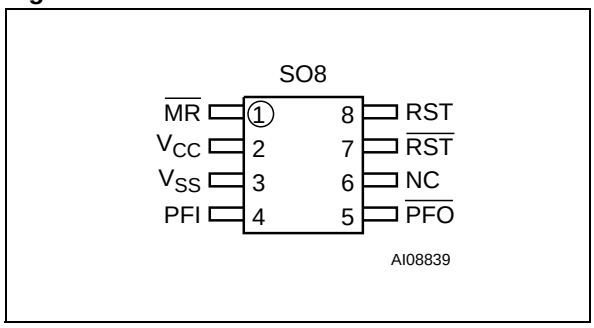
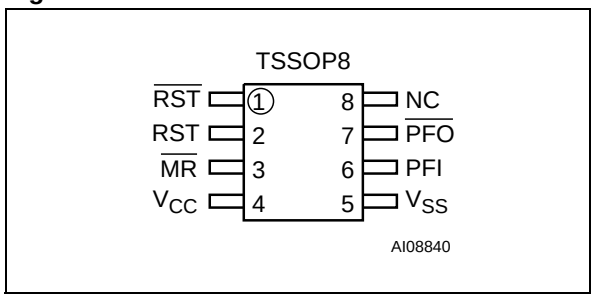


Figure 7. STM708T/S/R TSSOP8 Connections



Pin Descriptions

$\overline{MR}$. A logic low on $\overline{MR}$ asserts the reset output. Reset remains asserted as long as $\overline{MR}$ is low and for t_{rec} after $\overline{MR}$ returns high. This active-low input has an internal pull-up. It can be driven from a TTL or CMOS logic line, or shorted to ground with a switch. Leave open if unused.

WDI. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and reset (or $\overline{WDO}$) is triggered. The internal watchdog timer clears while reset is asserted or when WDI sees a rising or falling edge.

The watchdog function cannot be disabled by allowing the WDI pin to float.

$\overline{WDO}$. $\overline{WDO}$ goes low when a transition does not occur on WDI within 1.6sec, and remains low until a transition occurs on WDI (indicating the watchdog interrupt has been serviced). $\overline{WDO}$ also goes low when V_{CC} falls below the reset threshold; however, unlike the reset output, $\overline{WDO}$ goes high as soon as V_{CC} exceeds the reset threshold.

Note: For those devices with a $\overline{WDO}$ output, a watchdog timeout will not trigger reset unless $\overline{WDO}$ is connected to $\overline{MR}$.

$\overline{RST}$. Pulses low for t_{rec} when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is a logic low. It remains low for t_{rec} after either V_{CC} rises above the reset threshold, the watchdog triggers a reset, or $\overline{MR}$ goes from low to high.

RST. Pulses high for t_{rec} when triggered, and stays high whenever V_{CC} is above the reset threshold or when $\overline{MR}$ is a logic high. It remains high for t_{rec} after either V_{CC} falls below the reset threshold, the watchdog triggers a reset, or $\overline{MR}$ goes from high to low.

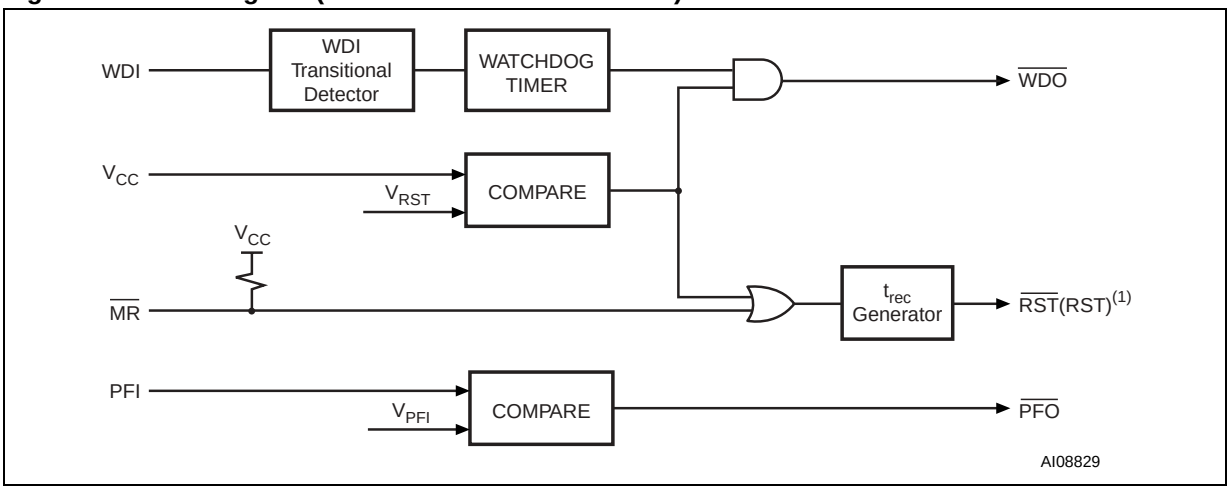
PFI. When PFI is less than V_{PFI}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high. Connect to ground if unused.

$\overline{PFO}$. When PFI is less than V_{PFI}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high. Leave open if unused.

Table 3. Pin Description

Pin						Name	Function
STM706P		STM706T/S/R		STM708T/S/R			
SO8	TSSOP8	SO8	TSSOP8	SO8	TSSOP8		
1	3	1	3	1	3	$\overline{MR}$	Push-button Reset Input
6	8	6	8	–	–	WDI	Watchdog Input
8	2	8	2	–	–	$\overline{WDO}$	Watchdog Output
–	–	7	1	7	1	$\overline{RST}$	Active-Low Reset Output
7	1	–	–	8	2	RST	Active-High Reset Output
2	4	2	4	2	4	V_{CC}	Supply Voltage
4	6	4	6	4	6	PFI	PFI Power-fail Input
5	7	5	7	5	7	$\overline{PFO}$	$\overline{PFO}$ Power-fail Output
3	5	3	5	3	5	V_{SS}	Ground
–	–	–	–	6	8	NC	No Connect

Figure 8. Block Diagram (STM706T/S/R and STM706P)



Note: 1. For STM706P only.

Figure 9. Block Diagram (STM708T/S/R)

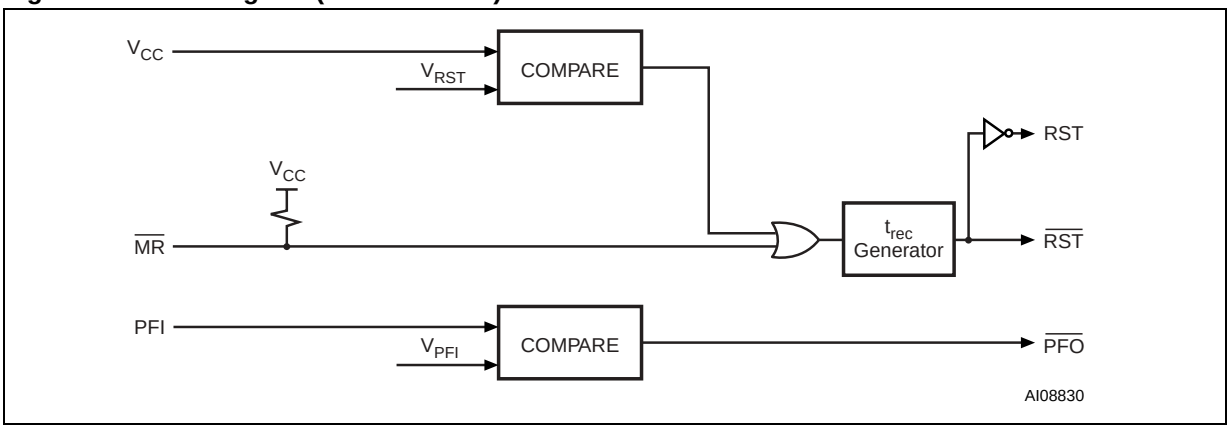
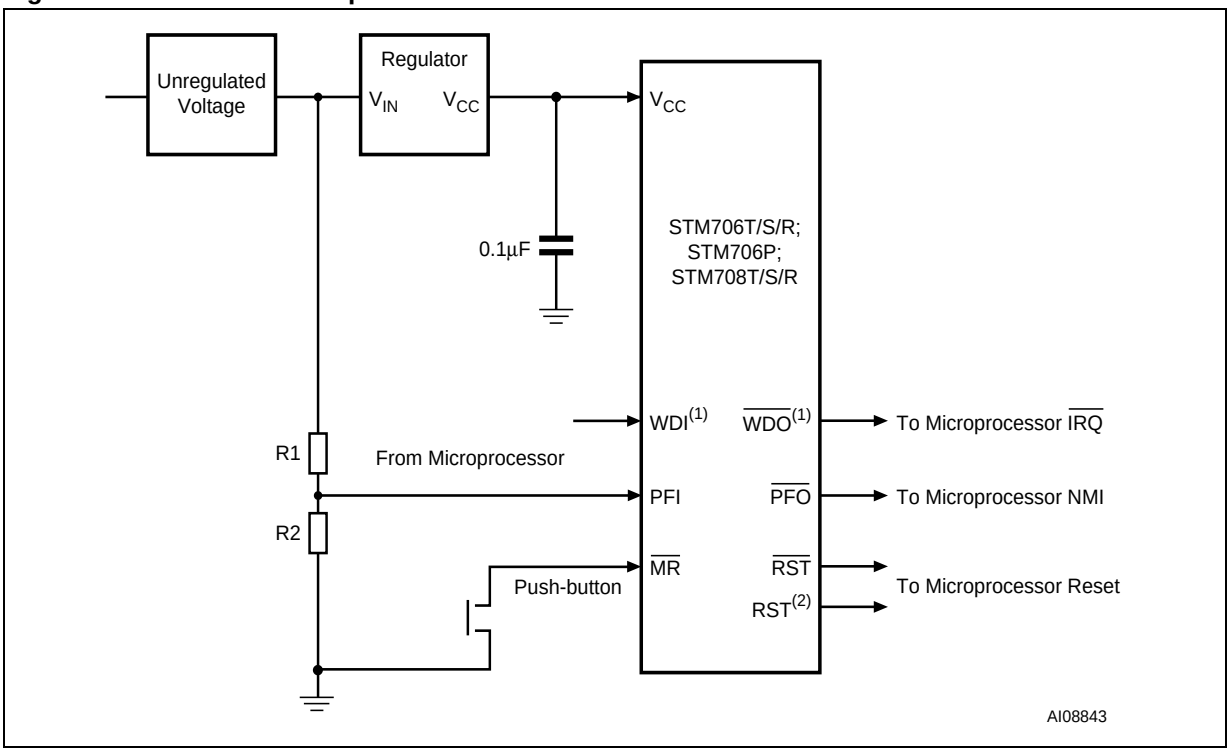


Figure 10. Hardware Hookup



Note: 1. For STM706T/S/R and STM706P.
2. For STM706P and STM708T/S/R.

OPERATION

Reset Output

The STM70x Supervisor asserts a reset signal to the MCU whenever V_{CC} goes below the reset threshold (V_{RST}), a watchdog time-out occurs (if $\overline{WDO}$ is connected to $\overline{MR}$), or when the Push-button Reset Input ($\overline{MR}$) is taken low. $\overline{RST}$ is guaranteed to be a logic low (logic high for STM706P and STM708T/S/R) for $V_{CC} < V_{RST}$ down to V_{CC} =1V for T_A = 0°C to 85°C.

During power-up, once V_{CC} exceeds the reset threshold an internal timer keeps $\overline{RST}$ low for the reset time-out period, t_{rec}. After this interval $\overline{RST}$ returns high.

If V_{CC} drops below the reset threshold, $\overline{RST}$ goes low. Each time $\overline{RST}$ is asserted, it stays low for at least the reset time-out period (t_{rec}). Any time V_{CC} goes below the reset threshold the internal timer clears. The reset timer starts when V_{CC} returns above the reset threshold.

Push-button Reset Input

A logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for t_{rec} (see Figure 29., page 19) after it returns high. The $\overline{MR}$ input has an internal 40kΩ pull-up resistor, allowing it to be left open if not used. This input can be driven with TTL/CMOS-logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1µF capacitor from $\overline{MR}$ to GND to provide additional noise immunity. $\overline{MR}$ may float, or be tied to V_{CC} when not used.

Watchdog Input (STM706T/S/R and STM706P)

The watchdog timer can be used to detect an out-of-control MCU. If the MCU does not toggle the Watchdog Input (WDI) within t_{WD} (1.6sec), the Watchdog Output pin ($\overline{WDO}$) is asserted. The internal 1.6sec timer is cleared by either:

1. a reset pulse, or
2. by toggling WDI (high-to-low or low-to-high), which can detect pulses as short as 50ns.

See Figure 30., page 19 for STM706T/S/R and STM706P.

The timer remains cleared and does not count for as long as reset is asserted. As soon as reset is released, the timer starts counting.

Watchdog Output (STM706T/S/R and STM706P)

When V_{CC} drops below the reset threshold, $\overline{WDO}$ will go low even if the watchdog timer has not yet timed out. However, unlike the reset output, $\overline{WDO}$ goes high as soon as V_{CC} exceeds the reset threshold. $\overline{WDO}$ may be used to generate a reset pulse by connecting it to the $\overline{MR}$ input.

Power-fail Input/Output

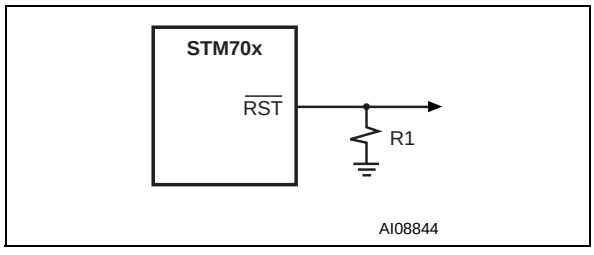
The Power-fail Input (PFI) is compared to an internal reference voltage (independent from the V_{RST} comparator). If PFI is less than the power-fail threshold (V_{PFI}), the Power-Fail Output ($\overline{PFO}$) will go low. This function is intended for use as an undervoltage detector to signal a failing power supply. Typically PFI is connected through an external voltage divider (see Figure 10., page 8) to either the unregulated DC input (if it is available) or the regulated output of the V_{CC} regulator. The voltage divider can be set up such that the voltage at PFI falls below V_{PFI} several milliseconds before the regulated V_{CC} input to the STM70x or the microprocessor drops below the minimum operating voltage.

If the comparator is unused, PFI should be connected to V_{SS} and $\overline{PFO}$ left unconnected. $\overline{PFO}$ may be connected to $\overline{MR}$ on the STM70x so that a low voltage on PFI will generate a reset output.

Ensuring a Valid Reset Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the state of the $\overline{RST}$ output can no longer be guaranteed, and becomes essentially an open circuit. If a high value pull-down resistor is added to the $\overline{RST}$ pin, the output will be held low during this condition. A resistor value of approximately 100kΩ will be large enough to not load the output under operating conditions, but still sufficient to pull $\overline{RST}$ to ground during this low voltage condition (see Figure 11).

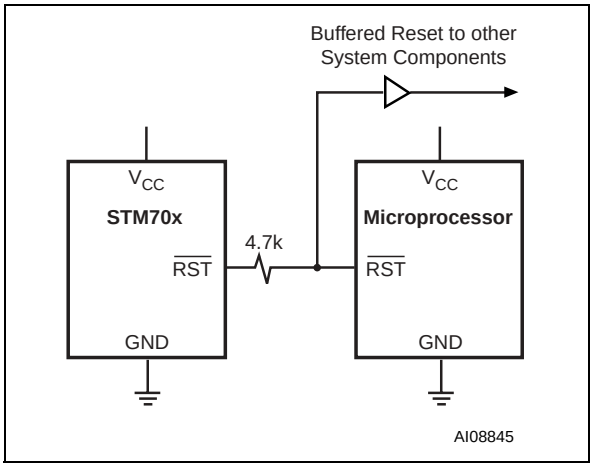
Figure 11. Reset Output Valid to Ground Circuit



Interfacing to Microprocessors with Bi-directional Reset Pins

Microprocessors with bi-directional reset pins can contend with the STM70x reset output. For example, if the reset output is driven high and the micro wants to pull it low, signal contention will result. To prevent this from occurring, connect a 4.7kΩ resistor between the reset output and the micro's reset I/O as in Figure 12.

Figure 12. Interfacing to Microprocessors with Bi-directional Reset I/O



TYPICAL OPERATING CHARACTERISTICS

Note: Typical values are at T_A = 25°C.

Figure 13. Supply Current vs. Temperature (no load)

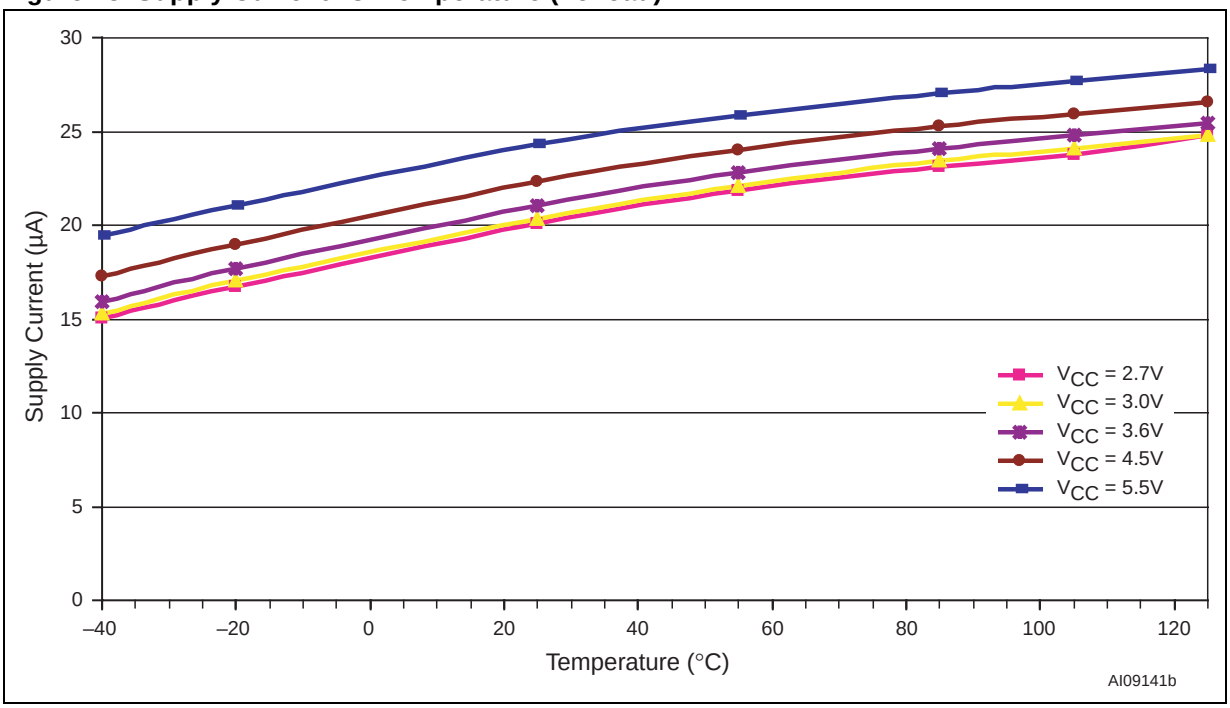


Figure 14. V_{PFI} Threshold vs. Temperature

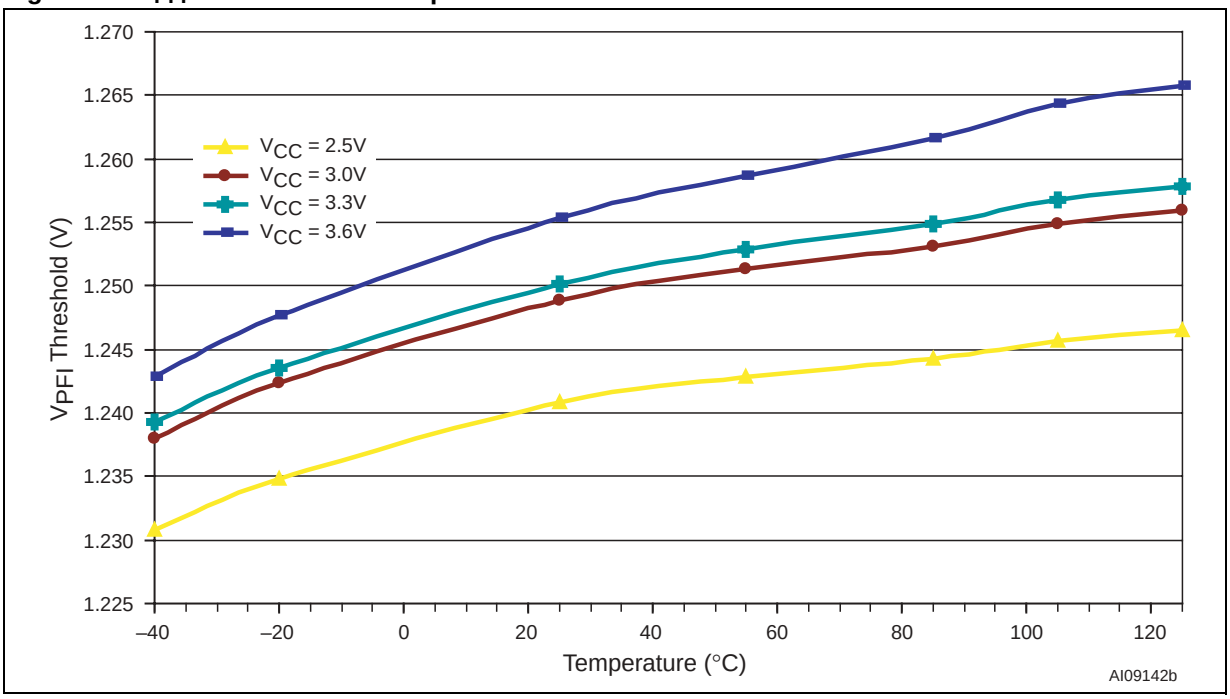


Figure 15. Reset Comparator Propagation Delay vs. Temperature

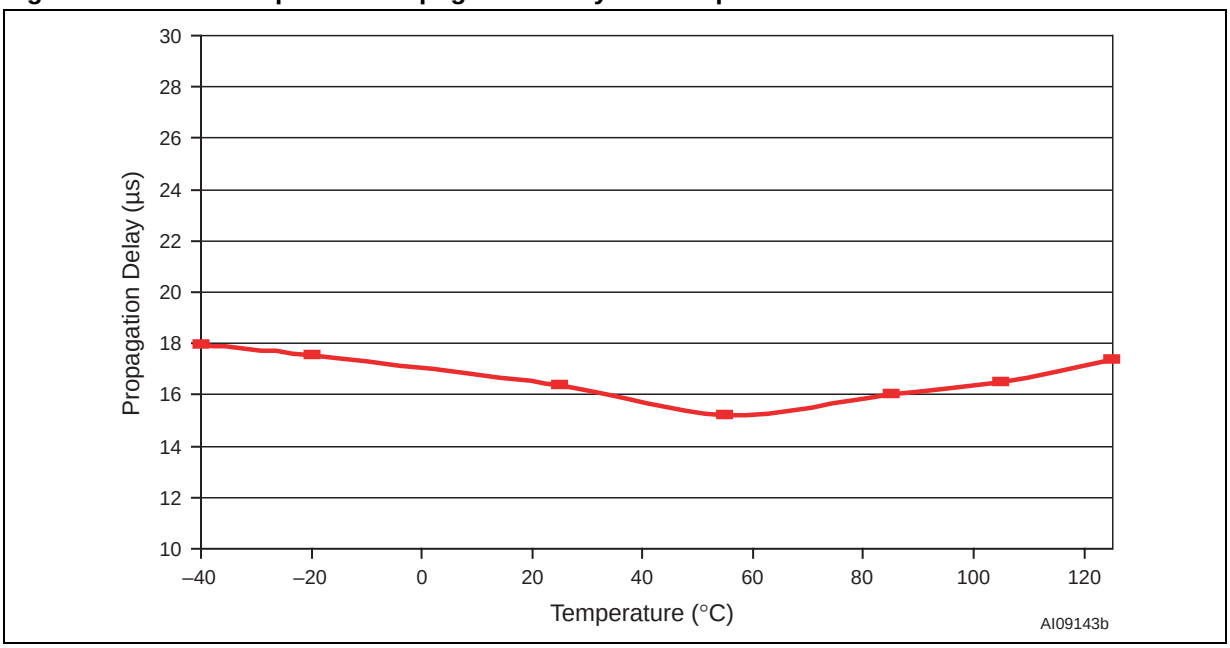


Figure 16. Power-up t_{rec} vs. Temperature

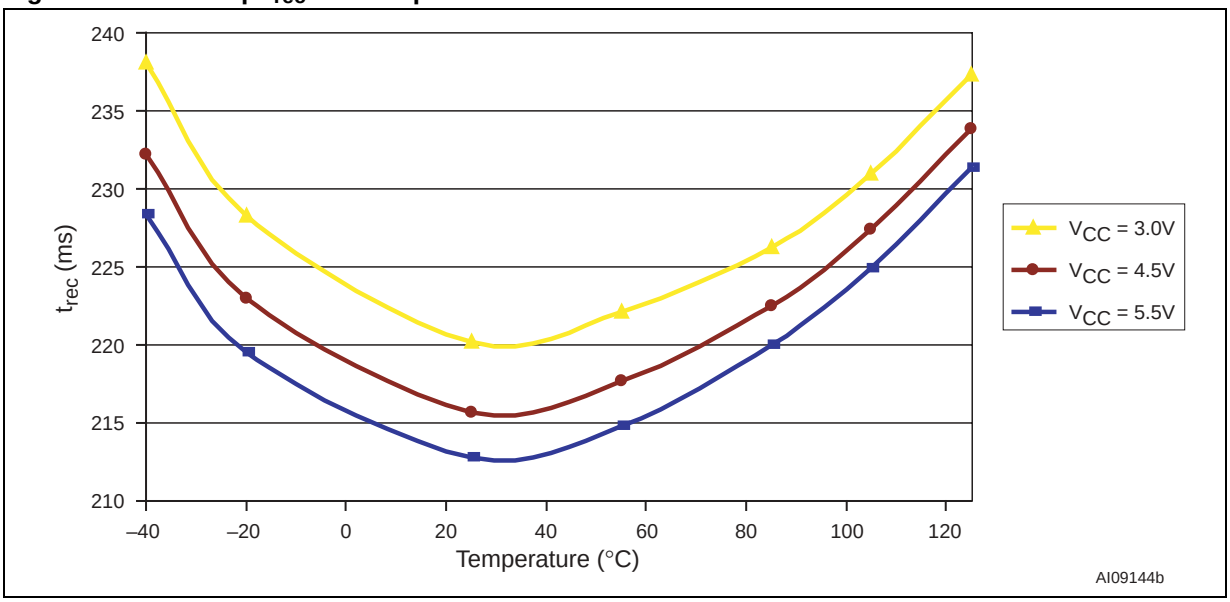


Figure 17. Normalized Reset Threshold vs. Temperature

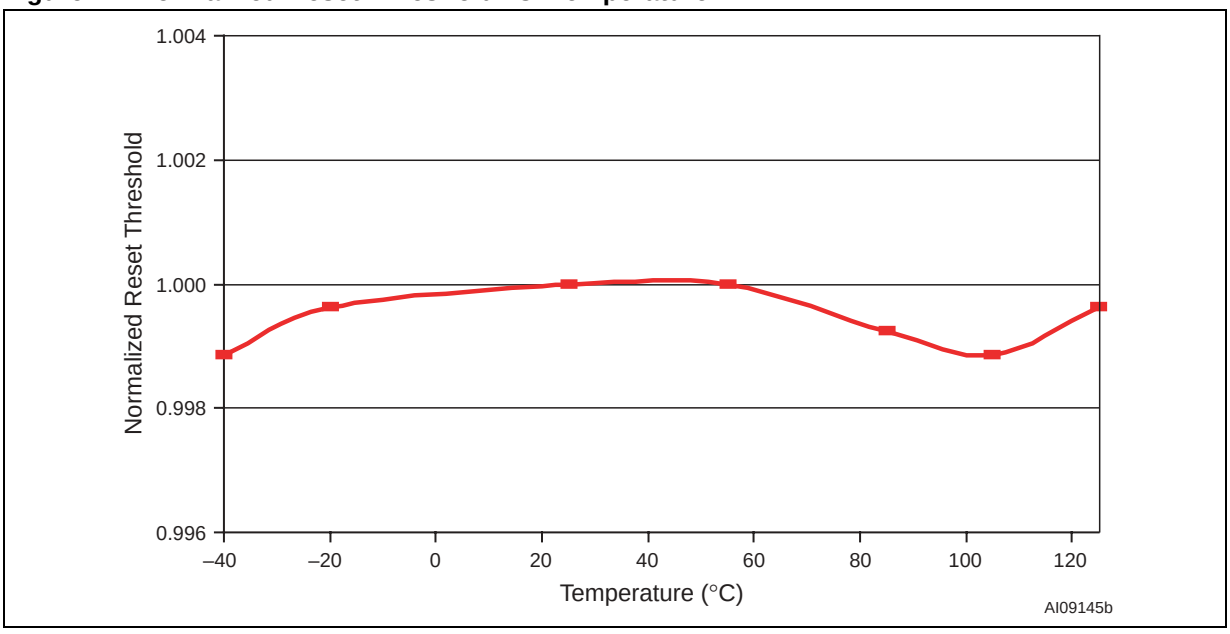


Figure 18. Watchdog Time-out Period vs. Temperature

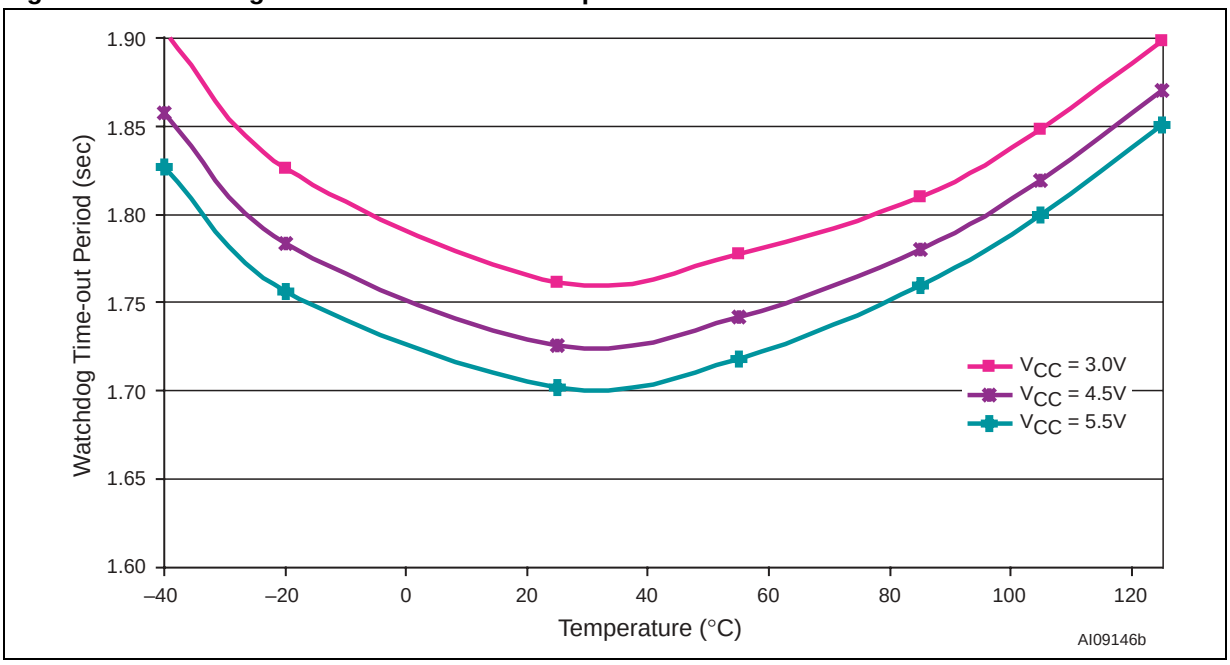


Figure 19. PFI to $\overline{\text{PFO}}$ Propagation Delay vs. Temperature

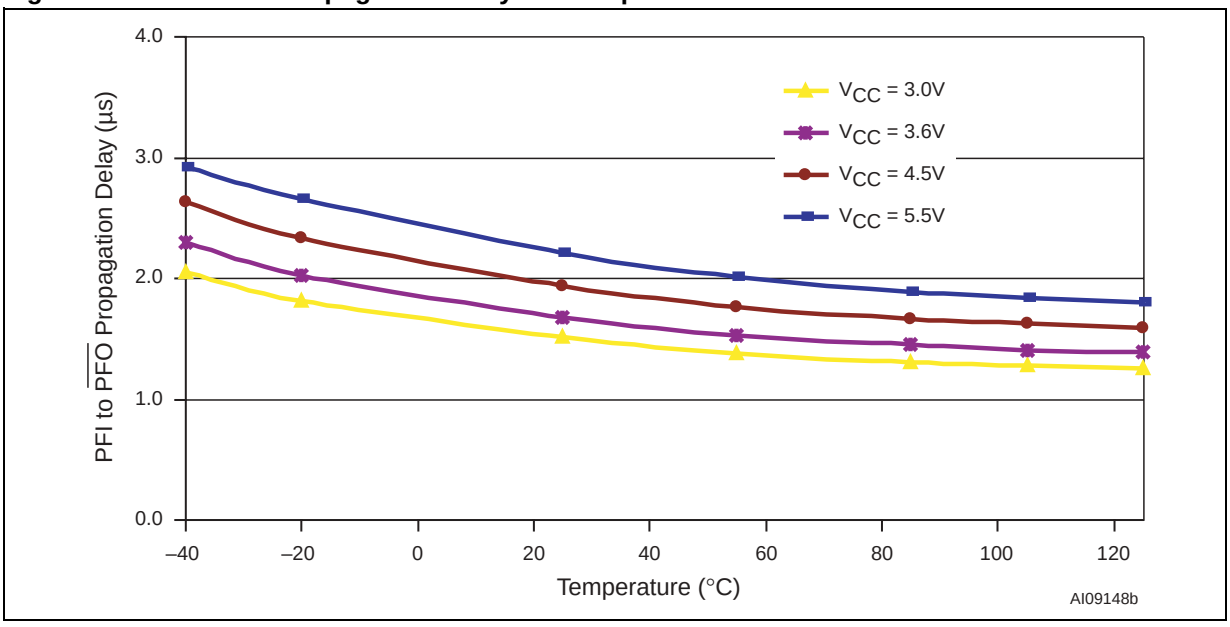


Figure 20. Output Voltage vs. Load Current (V_{CC} = 5V; V_{BAT} = 2.8V; T_A = 25°C)

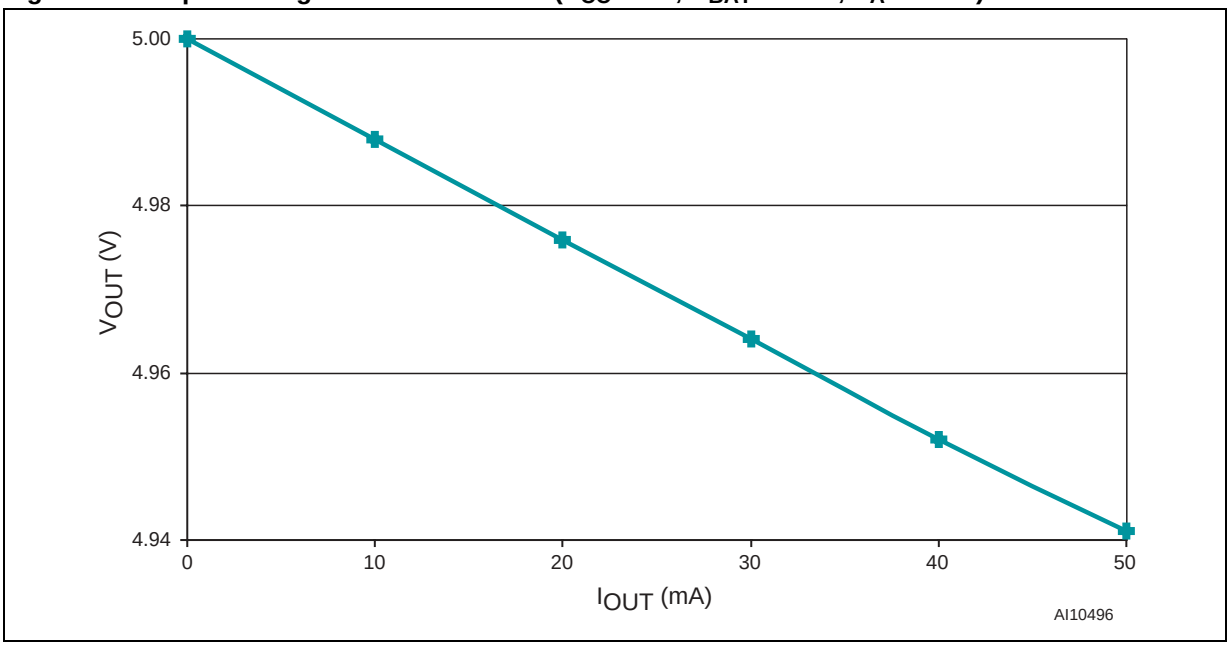


Figure 21. Output Voltage vs. Load Current (V_{CC} = 0V; V_{BAT} = 2.8V; T_A = 25°C)

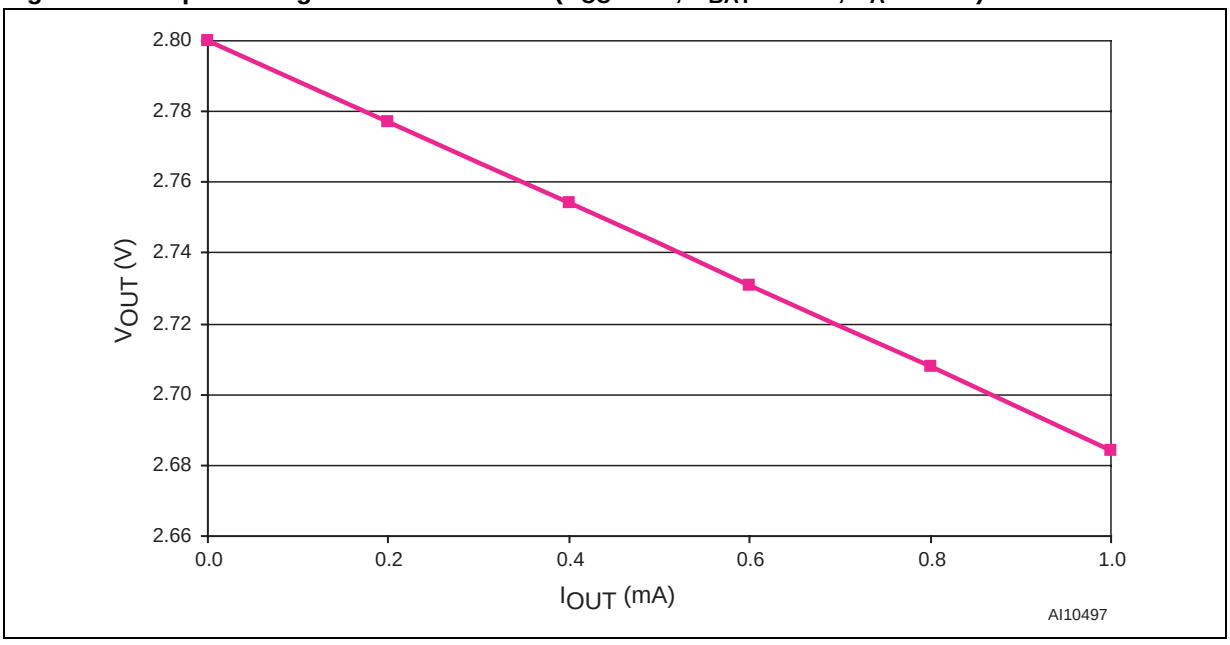


Figure 22. $\overline{RST}$ Output Voltage vs. Supply Voltage

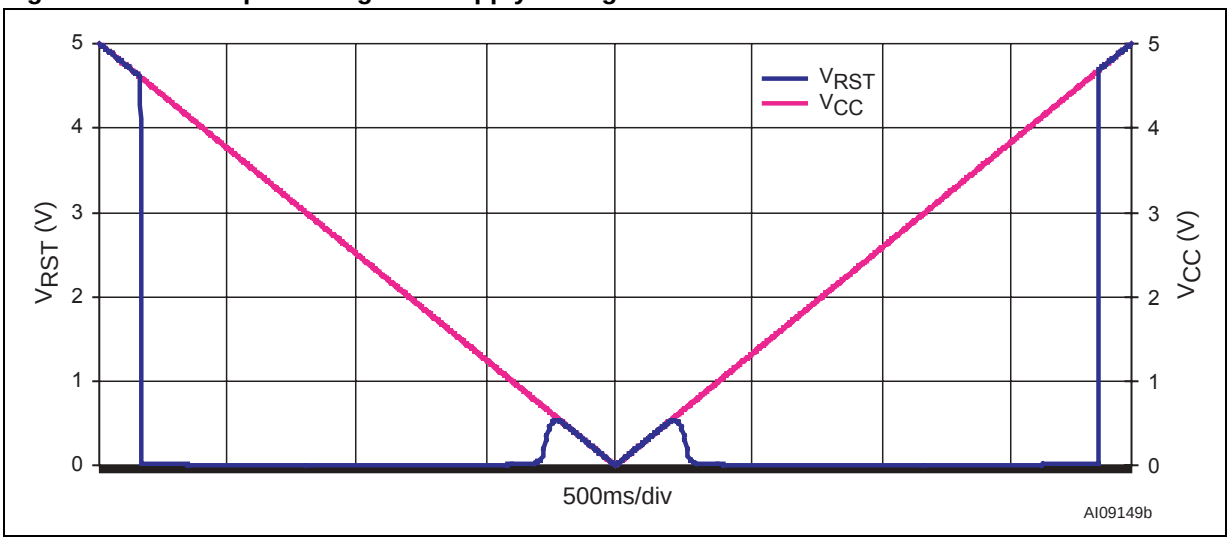


Figure 23. RST Output Voltage vs. Supply Voltage

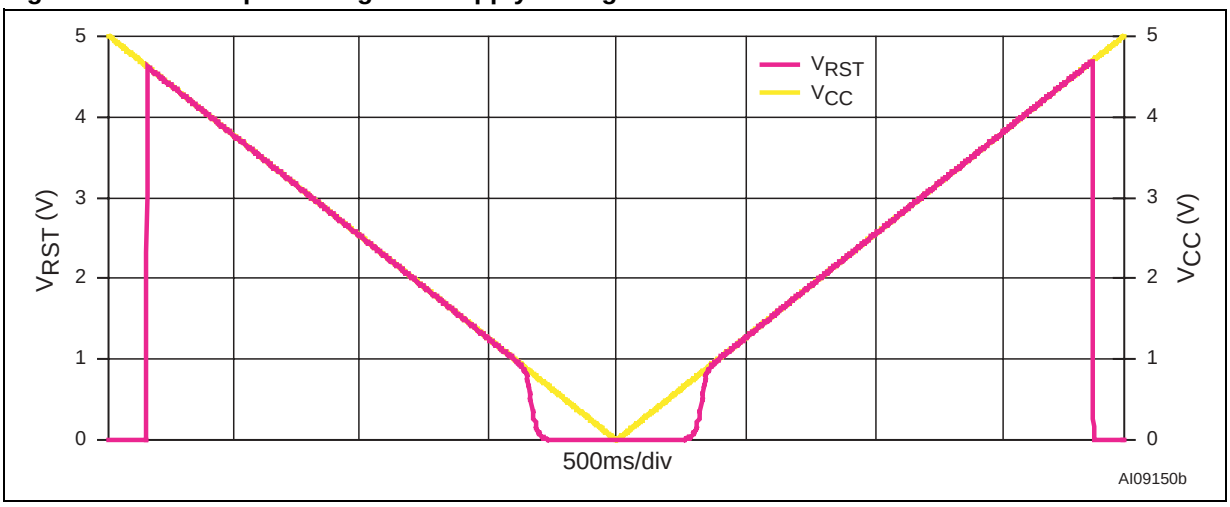


Figure 24. Power-fail Comparator Response Time (Assertion)

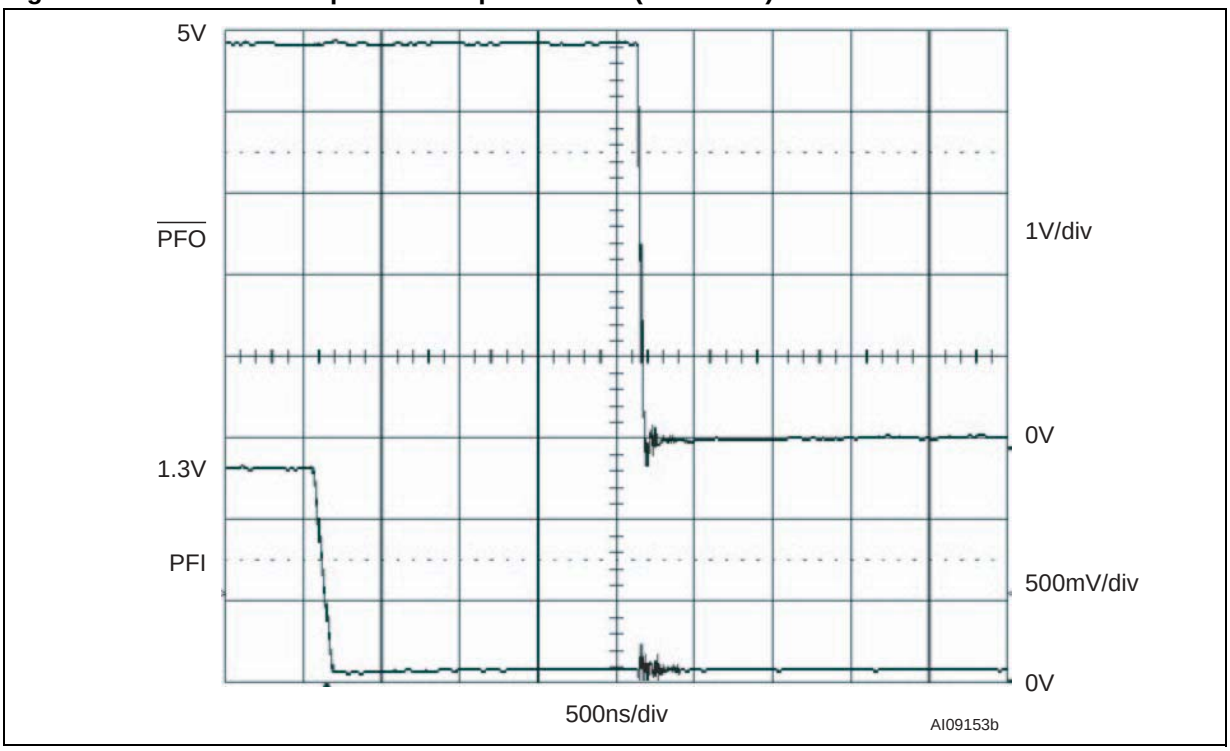


Figure 25. Power-fail Comparator Response Time (De-Assertion)

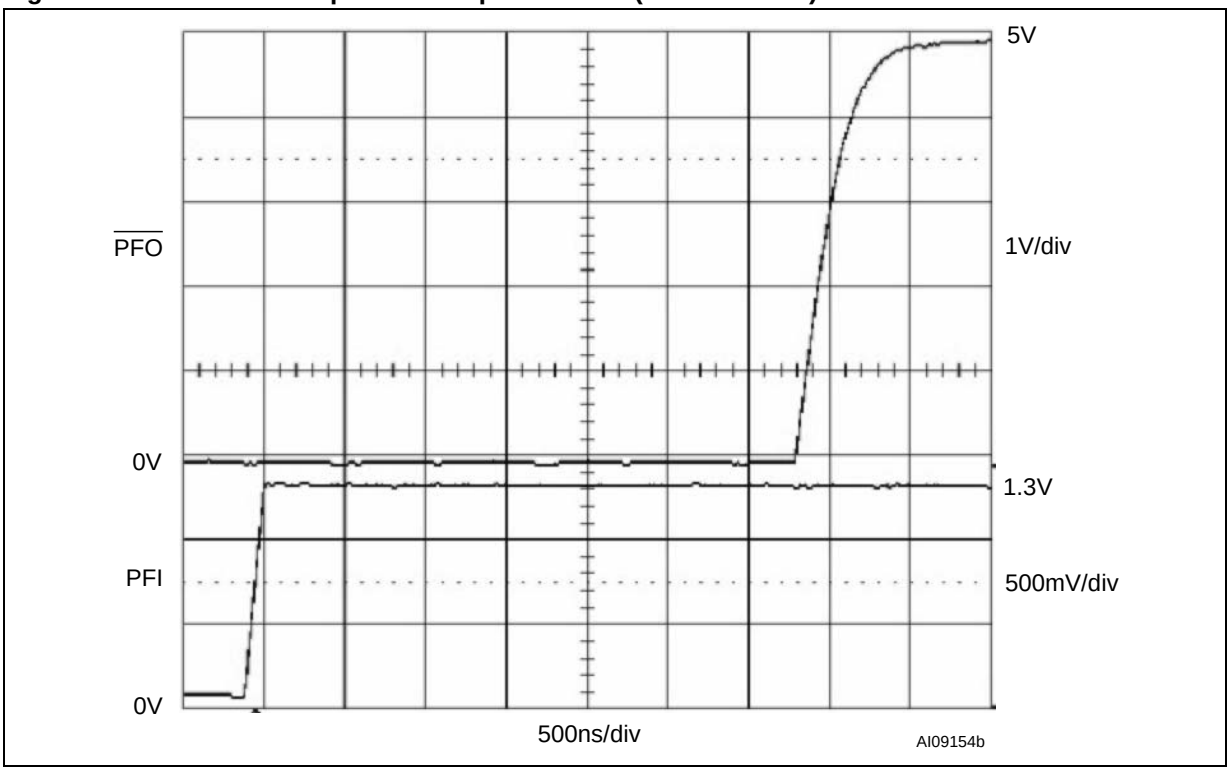
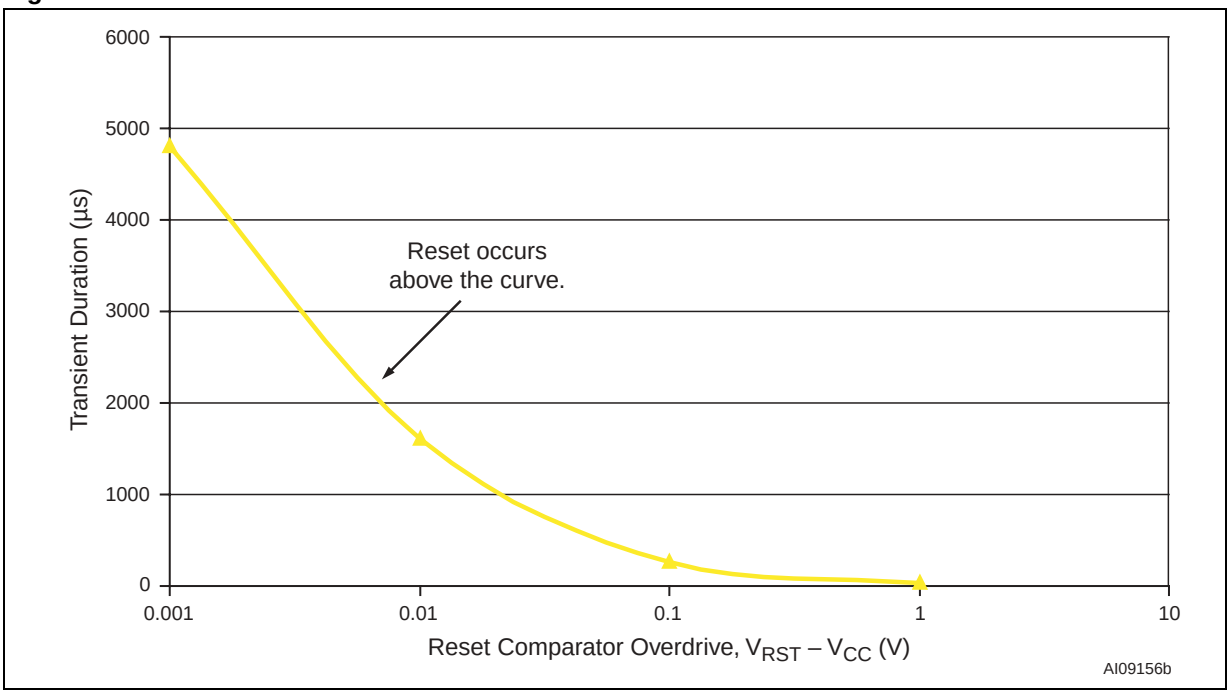


Figure 26. Maximum Transient Duration vs. Reset Threshold Overdrive



MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature (V_{CC} Off)	–55 to 150	°C
T_{SLD}(1)	Lead Solder Temperature for 10 seconds	260	°C
V_{IO}	Input or Output Voltage	–0.3 to V_{CC} +0.3	V
V_{CC}	Supply Voltage	–0.3 to 7.0	V
I_O	Output Current	20	mA
P_D	Power Dissipation	320	mW

Note: 1. Reflow at peak temperature of 255°C to 260°C for < 30 seconds (total thermal budget not to exceed 180°C for between 90 to 150 seconds).

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 5, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 5. Operating and AC Measurement Conditions

Parameter	STM70x	Unit
V_{CC} Supply Voltage	1.0 to 5.5	V
Ambient Operating Temperature (T_A)	–40 to 85	°C
Input Rise and Fall Times	≤ 5	ns
Input Pulse Voltages	0.2 to 0.8V_{CC}	V
Input and Output Timing Ref. Voltages	0.3 to 0.7V_{CC}	V

Figure 27. AC Testing Input/Output Waveforms

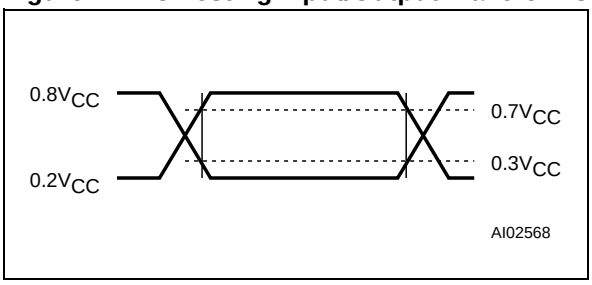


Figure 28. Power-fail Comparator Waveform

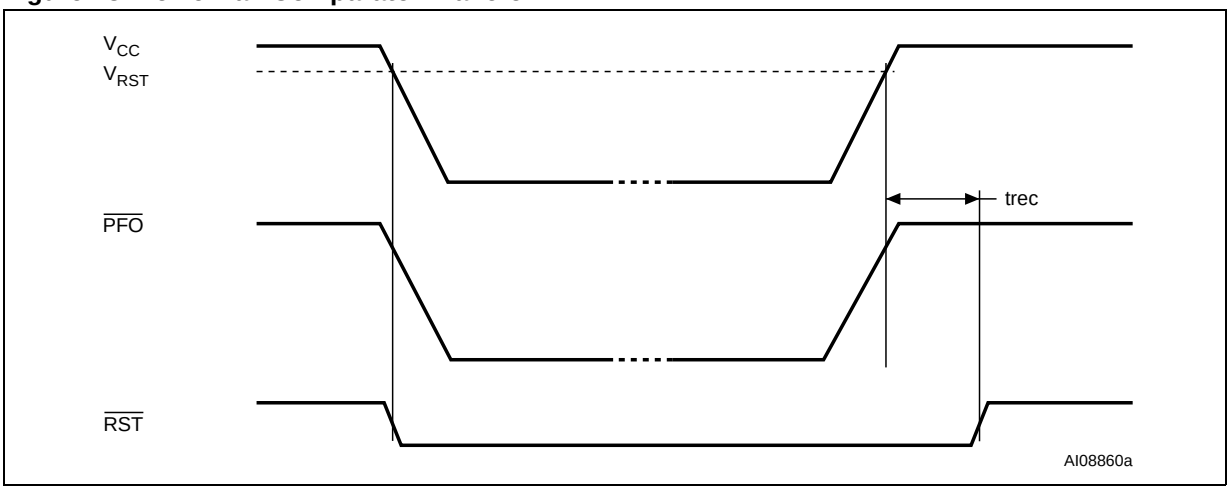
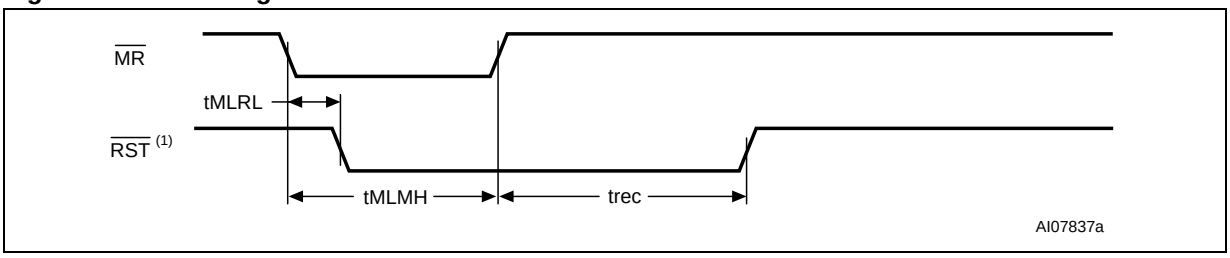


Figure 29. $\overline{MR}$ Timing Waveform



Note: 1. RST for STM706P and STM708T/S/R.

Figure 30. Watchdog Timing (STM706T/S/R and STM706P)

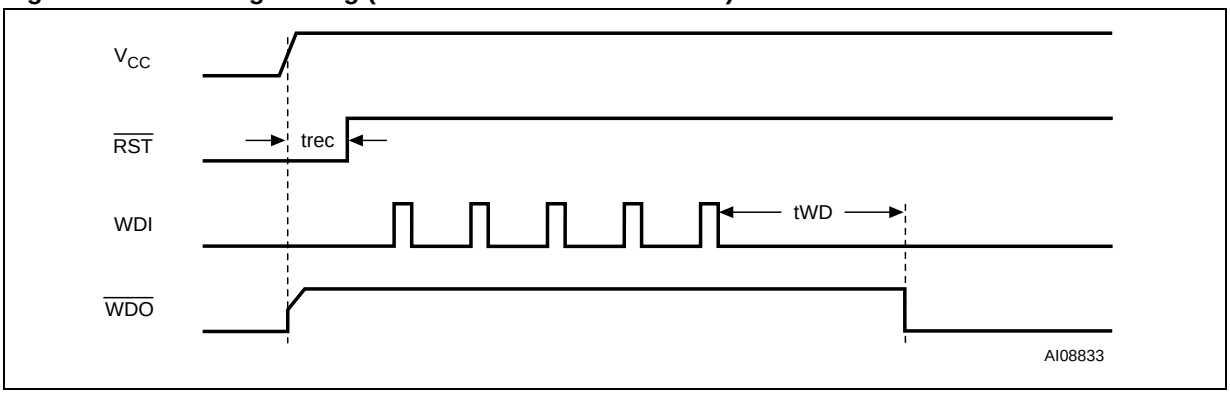


Table 6. DC and AC Characteristics

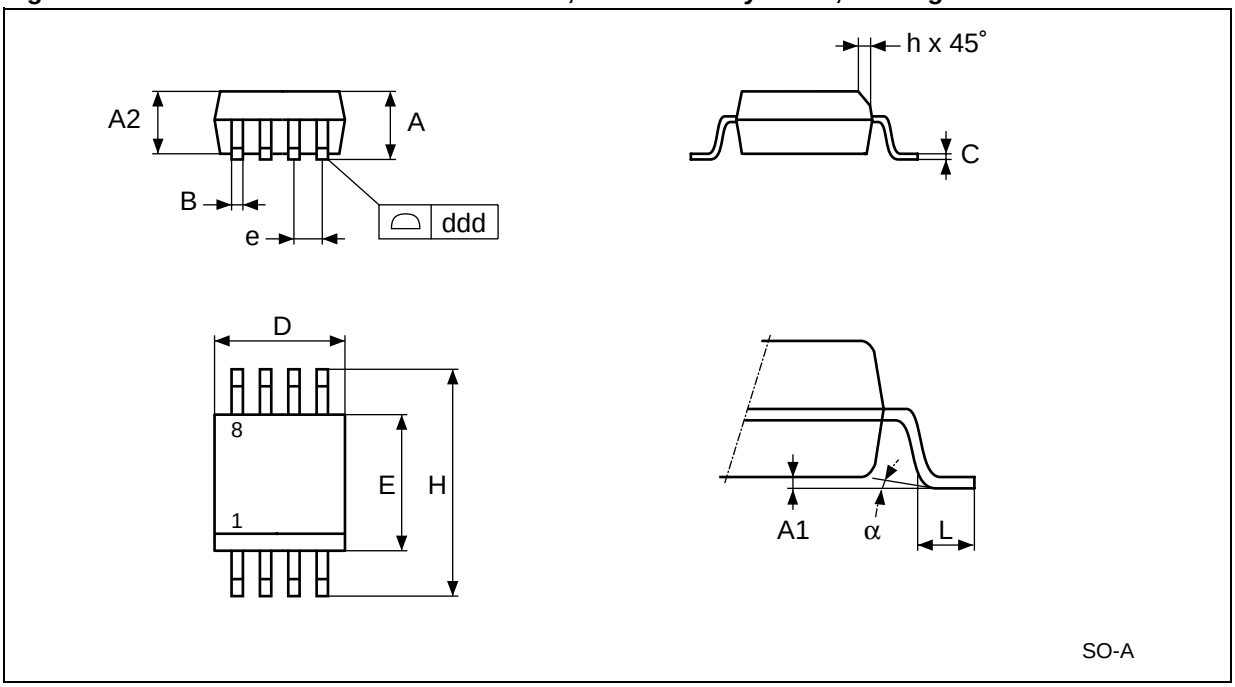
Sym	Alter-native	Description	Test Condition(1)	Min	Typ	Max	Unit
V_{CC}		Operating Voltage		1.2(2)		5.5	V
I_{CC}		V_{CC} Supply Current	V_{CC} < 3.6V		35	50	µA
			V_{CC} < 5.5V		40	60	µA
I_{LI}		Input Leakage Current (WDI)	0V = V_{IN} = V_{CC}	–1		+1	µA
		Input Leakage Current (PFI)	0V = V_{IN} = V_{CC}	–25	2	+25	nA
		Input Leakage Current ($\overline{MR}$)	V_{RST} (max) < V_{CC} < 3.6V	25	80	250	µA
			4.5V < V_{CC} < 5.5V	75	125	300	µA
V_{IH}		Input High Voltage ($\overline{MR}$)	4.5V < V_{CC} < 5.5V	2.0			V
			V_{RST} (max) < V_{CC} < 3.6V	0.7V_{CC}			V
V_{IH}		Input High Voltage (WDI)	V_{RST} (max) < V_{CC} < 5.5V	0.7V_{CC}			V
V_{IL}		Input Low Voltage ($\overline{MR}$)	4.5V < V_{CC} < 5.5V			0.8	V
			V_{RST} (max) < V_{CC} < 3.6V			0.6	V
V_{IL}		Input Low Voltage (WDI)	V_{RST} (max) < V_{CC} < 5.5V			0.3V_{CC}	V

Sym	Alter-native	Description	Test Condition(1)	Min	Typ	Max	Unit
V_{OL}		Output Low Voltage ($\overline{PFO}$, $\overline{RST}$, RST, $\overline{WDO}$)	$V_{CC} = V_{RST}$ (max), I_{SINK} = 3.2mA			0.3	V
V_{OL}		Output Low Voltage ($\overline{RST}$)	I_{SINK} = 50µA, V_{CC} = 1.0V, T_A = 0°C to 85°C			0.3	V
			I_{SINK} = 100µA, V_{CC} = 1.2V			0.3	V
V_{OH}		Output High Voltage ($\overline{RST}$, RST, $\overline{WDO}$)	I_{SOURCE} = 1mA, $V_{CC} = V_{RST}$ (max)	2.4			V
		Output High Voltage ($\overline{PFO}$)	I_{SOURCE} = 75µA, $V_{CC} = V_{RST}$ (max)	$0.8V_{CC}$			V
Power-fail Comparator							
V_{PFI}		PFI Input Threshold	PFI Falling (STM70xP/R, V_{CC} = 3.0V; STM70xS/T, V_{CC} = 3.3V)	1.20	1.25	1.30	V
t_{PFD}		PFI to $\overline{PFO}$ Propagation Delay			2		µs
Reset Thresholds							
V_{RST}		Reset Threshold(3)	STM706P/70xR	2.55	2.63	2.70	V
			STM70xS	2.85	2.93	3.00	V
			STM70xT	3.00	3.08	3.15	V
		Reset Threshold Hysteresis			20		mV
t_{rec}		$\overline{RST}$ Pulse Width		140	200	280	ms
Push-button Reset Input							
t_{MLMH}	t_{MR}	$\overline{MR}$ Pulse Width	V_{RST} (max) < V_{CC} < 3.6V	500			ns
			4.5V < V_{CC} < 5.5V	150			ns
t_{MLRL}	t_{MRD}	$\overline{MR}$ to $\overline{RST}$ Output Delay	V_{RST} (max) < V_{CC} < 3.6V			750	ns
			4.5V < V_{CC} < 5.5V			250	ns
Watchdog Timer (STM706T/S/R and STM706P)							
t_{WD}		Watchdog Timeout Period	STM706P/70xR, V_{CC} = 3.0V	1.12	1.60	2.24	s
			STM70xS/70XT, V_{CC} = 3.3V				
		WDI Pulse Width	4.5V < V_{CC} < 5.5V	50			ns
			V_{RST} (max) < V_{CC} < 3.6V	100			ns

Note: 1. Valid for Ambient Operating Temperature: T_A = –40 to 85°C; $V_{CC} = V_{RST}$ (max) to 5.5V (except where noted).
2. V_{CC} (min) = 1.0V for T_A = 0°C to +85°C.
3. For V_{CC} falling.

PACKAGE MECHANICAL

Figure 31. SO8 – 8-lead Plastic Small Outline, 150 mils body width, Package Mechanical

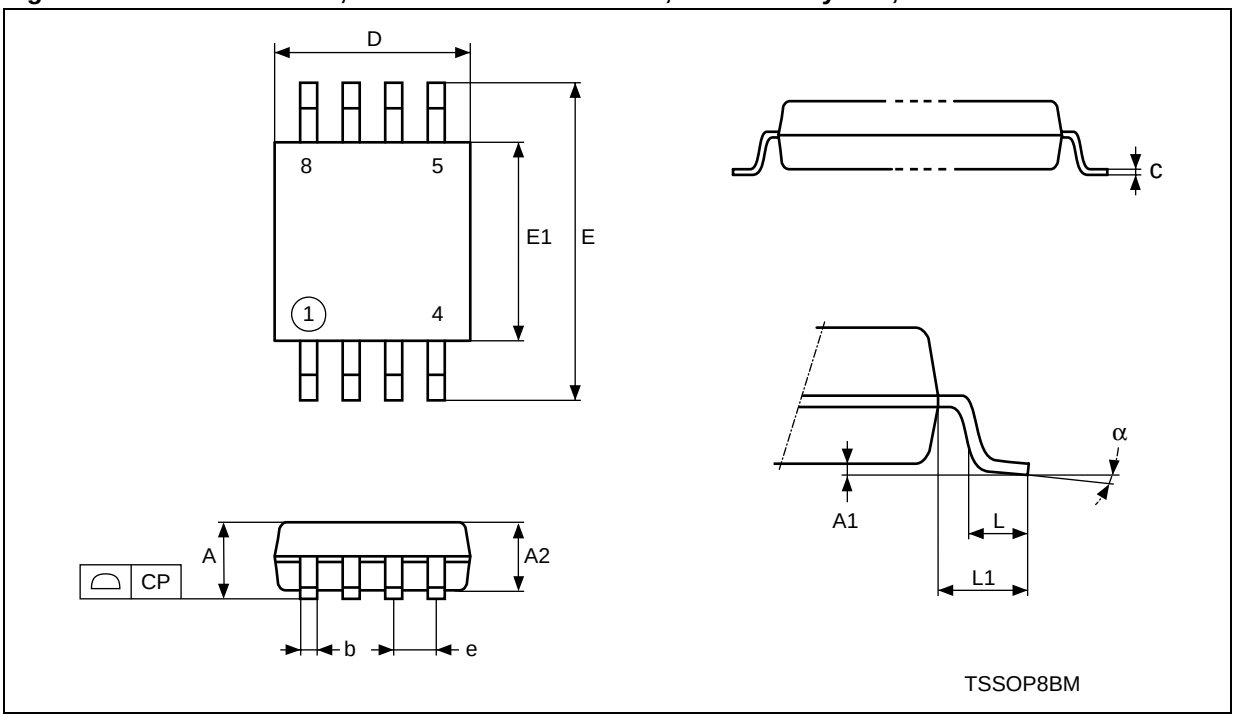


Note: Drawing is not to scale.

Table 7. SO8 – 8-lead Plastic Small Outline, 150 mils body width, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	–	1.35	1.75	–	0.053	0.069
A1	–	0.10	0.25	–	0.004	0.010
B	–	0.33	0.51	–	0.013	0.020
C	–	0.19	0.25	–	0.007	0.010
D	–	4.80	5.00	–	0.189	0.197
ddd	–	–	0.10	–	–	0.004
E	–	3.80	4.00	–	0.150	0.157
e	1.27	–	–	0.050	–	–
H	–	5.80	6.20	–	0.228	0.244
h	–	0.25	0.50	–	0.010	0.020
L	–	0.40	0.90	–	0.016	0.035
α	–	0°	8°	–	0°	8°
N	8			8		

Figure 32. TSSOP8 – 8-lead, Thin Shrink Small Outline, 3x3mm body size, Outline



Note: Drawing is not to scale.

Table 8. TSSOP8 – 8-lead, Thin Shrink Small Outline, 3x3mm body size, Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.10	–	–	0.043
A1	–	0.05	0.15	–	0.002	0.006
A2	0.85	0.75	0.95	0.034	0.030	0.037
b	–	0.25	0.40	–	0.010	0.016
c	–	0.13	0.23	–	0.005	0.009
CP	–	–	0.10	–	–	0.004
D	3.00	2.90	3.10	0.118	0.114	0.122
e	0.65	–	–	0.026	–	–
E	4.90	4.65	5.15	0.193	0.183	0.203
E1	3.00	2.90	3.10	0.118	0.114	0.122
L	0.55	0.40	0.70	0.022	0.016	0.030
L1	0.95	–	–	0.037	–	–
α	–	0°	6°	–	0°	6°
N	8			8		

PART NUMBERING

Table 9. Ordering Information Scheme

Example: STM706 T M 6 E

Device Type

STM706

STM708

Reset Threshold Voltage

T: 3.00V ≤ V_{RST} ≤ 3.15V

S: 2.88V ≤ V_{RST} ≤ 3.00V

R, STM706P: 2.59V ≤ V_{RST} ≤ 2.70V

Package

M = SO8

DS = TSSOP8

Temperature Range

6 = –40 to 85°C

Shipping Method

E = Tubes

F = Tape & Reel

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

Table 10. Marking Description

Part Number	Reset Threshold	Package	Topside Marking
STM706P	2.63V	SO8	706P
		TSSOP8	
STM706T	3.08V	SO8	706T
		TSSOP8	
STM706S	2.93V	SO8	706S
		TSSOP8	
STM706R	2.63V	SO8	706R
		TSSOP8	
STM708T	3.08V	SO8	708T
		TSSOP8	
STM708S	2.93V	SO8	708S
		TSSOP8	
STM708R	2.63V	SO8	708R
		TSSOP8	

REVISION HISTORY

Table 11. Document Revision History

Date	Version	Revision Details
October 2003	1.0	First Issue
12-Dec-03	2.0	Reformatted; update characteristics (Figure 2, 3, 8, 9, 10, 28, 29, 30; Table 6, 7, 8, 9)
16-Jan-04	2.1	Add Typical Operating Characteristics (Figure 13, 14, 15, 16, 17, 18, 19, 22, 23, 24, 25, 26)
09-Apr-04	3.0	Reformatted; update characteristics (Figure 15, 19, 22, 23, 26; Table 6)
25-May-04	4.0	Update characteristics (Table 3, 6)
02-Jul-04	5.0	Datasheet promoted; waveform corrected (Figure 28)
21-Sep-04	6.0	Clarify root part numbers; (Figure 2, 3, 4, 5, 6, 7, 8, 9, 10, 30; Table 1, 3, 6, 9)
25-Feb-05	7.0	Update Typical Characteristics (Figure 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26)

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